WHAT IS CLAIMED IS:

1. A method of programming a non-volatile memory with a nitride tunneling layer, the non-volatile memory having a substrate, a nitride tunneling layer on the substrate, a charge-trapping layer on the nitride tunneling layer, a dielectric layer on the charge-rapping layer, a gate conductive layer on the dielectric layer, and a source region and a drain region in the substrate beside the gate conductive layer, and the method comprising the steps of:

applying a first voltage to the gate conductive layer and grounding the substrate to turn on a channel between the source region and the drain region; and

applying a second voltage to the drain region and grounding the source region to induce a current in the channel and thereby to generate hot electrons in the channel, wherein the hot electrons are injected into the charge-trapping layer through the nitride tunneling layer.

2. The method of claim 1, wherein the first voltage ranges from about 6V to about 12V.

3. The method of claim 1, wherein the second voltage ranges from about 2.5V to about 5V.

4. The method of claim 1, wherein the first voltage and the second voltage are both lower than those adopted for programming a substrate-oxide-nitride-oxide-silicon (SONOS) memory having a same size as the non-volatile memory with the nitride tunneling layer.

5. A method of erasing a non-volatile memory with a nitride tunneling layer, the non-volatile memory having a substrate, a nitride tunneling layer on the substrate, a charge-trapping layer on the nitride tunneling layer, a dielectric layer on the charge-rapping layer, a gate conductive layer on the dielectric layer, and a source region and a drain region in the substrate beside the gate conductive layer, and the method comprising the steps of:

applying a first positive bias to the drain region, applying a second positive bias to the gate conductive layer, and grounding the source region and the substrate to generate hot electron holes in a channel region, wherein the hot electron holes are injected into the charge-trapping layer through the nitride tunneling layer.

6. The method of claim 5, wherein the first positive bias ranges from about 2V to about 5V.

7. The method of claim 5, wherein the second positive bias ranges from about 2.5V to about 5V.

8. The method of claim 5, wherein the first positive bias and the second positive bias are both lower than those adopted for erasing a substrate-oxide-nitride-oxide-silicon (SONOS) memory having a same size as the non-volatile memory with the nitride tunneling layer.